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[Kumar* *et al.*, 6(5): May, 2017]
IC™ Value: 3.00

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

IMPROVEMENT IN NOISE AND DELAY IN DOMINO CMOS LOGIC CIRCUIT

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DOI: Will get Assigned by IJESRT Team

ABSTRACT

New experiments are always welcomed in the field of chip designing in VLSI technology. VLSI is advanced innovation over solid state devices and is based on CMOS designing. CMOS is a combination of PMOS and NMOS. The CMOS technology is mostly used to reduce power dissipation in circuitry and to minimize the losses. Still a sufficient amount of noise is present, which can cause for distortion in transmitted signal and make the whole transmission spurious.

There are some known techniques which are used to minimize noise in any circuit i.e. keeper technique, pre-charge internal nodes and NMOS pull up transistor. The improvement over these three techniques is required so that noise could be more minimized and performance of circuitry can be increased. In this paper, experiments are done to add an additional part in the circuit to minimize the noise. The new improved circuit is named as 'HIGH SPEED MASTER OUTPUT KEEPER DOMINO TECHNIQUE' which minimize the noise up to great extent. All the experiment and calculations are done for logic gate using Tanner Tool EDA. The lowest noise present in AND gate was 1.75407 NV/HZ in old technique while it is minimize to 1.40310 NV/HZ in new technique.

KEYWORDS: simple domino logic, keeper domino logic, Smart output keeper domino technique, High speed master output keeper domino technique.

INTRODUCTION

DOMINO LOGIC TECHNIQUES

(A)BASIC DOMINO LOGIC- The problem in cascading conventional dynamic CMOS stages occurs when one or more inputs of a stage make a 1 to 0 transition during the evaluation phase. On the other hand, if we build a system by cascading domino CMOS logic gates as shown in Fig.1, all input transistors in subsequent logic blocks will be turned off during the pre-charge phase, since all buffer outputs are equal to 0. During the evaluation phase, each buffer output can make at most one transition Dynamic Logic Circuits (from 0 to 1), and thus each input of all subsequent logic stages can also make at most one (0 to 1) transition. In a cascade structure consisting of several such stages, the evaluation of each stage ripples the next stage evaluation, similar to a chain of dominos falling one after the other. The structure is hence called domino CMOS logic.

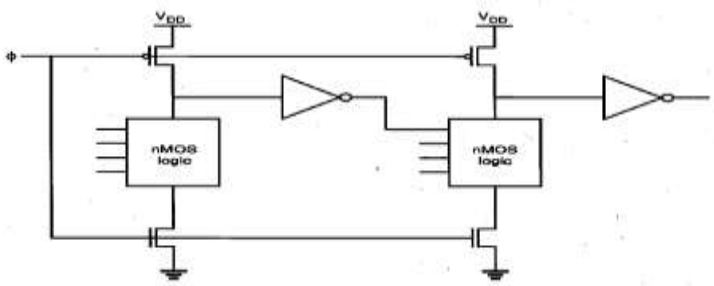

Fig 1

(B)KEEPER DOMINO LOGIC - Domino CMOS logic finds a wide variety of applications due to their high speed and low device count. However, this type of logic has the drawback of low noise immunity especially when

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compared to complementary CMOS logic. This is due to the leakage current and charge sharing. So, a PMOS keeper must be used in order to compensate for this leakage . The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper is tied to the ground. The use of keeper causes contention when the pull-down network is ON during the evaluation phase, resulting in slower overall gate performance. In wide fan-in gates designed using very deep submicron process technology, the large leakage current through the n-network necessitates a very strong keeper to retain the voltage at the dynamic node.

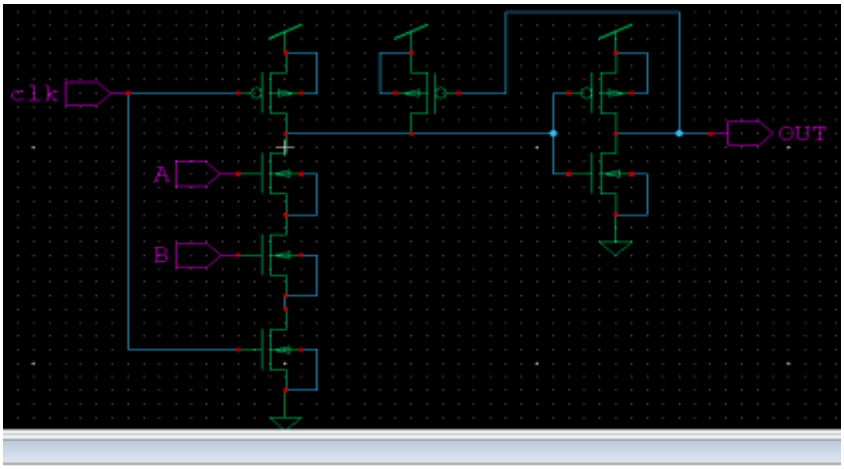

Fig. 2

(C) SMART OUTPUT KEEPER DOMINO TECHNIQUE- In digital circuits, there are logic 1 and logic 0. If voltage is above a particular voltage level , than it is consider as logic 1 and if it is below another voltage level , than it is called level 0. Noise generates in the circuit if the voltage lies between two level. In input, voltage above VIH is consider as logic 1 and voltage below VIL is consider as logic 0. Similarly, output has same logic 1 (above VOH) and logic 0 (below VOL). Clearly, the output voltage is greater than the VOL and less than the VOH is undefined region. Thus in this region we can't consider the output as either digital logic 0 or logic 1. This undefined region generate noise in the digital circuits.

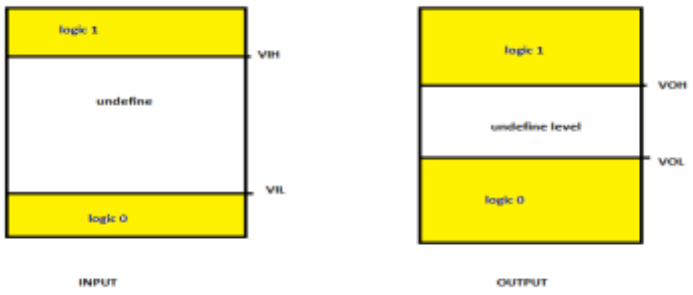

Fig. 3

In proposed technique, we make a master output keeper as when the dynamic node is HIGH, than output node should be less than VOL and when the dynamic node is LOW, than output node should be greater than VOH. Thus there will not be any output in the undefined region, clearly noise of the circuit is reduced.

In this technique , a simple cross coupled circuit is added in simple domino technique.
The working of the proposed technique is same as the simple domino logic except the smart output keeper logic.
CASE-1: When the dynamic node is HIGH, then output will be LOW because of the inverter circuit. Due to HIGH dynamic node, the NMOS of the smart keeper circuit is ON, and the output of the circuit is connected to ground. So we get the output as LOW.

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CASE-2:When the dynamic node is LOW, then output will be HIGH because of the inverter circuit. Due to LOW dynamic node, the PMOS of the smart keeper circuit is ON, and the output of the circuit is connected to VDD. So we get the output as HIGH.

Thus smart keeper keeps the output of the circuit at logic 1 or 0, but not at the undefined region. It is clear that the noise of the circuit is reduced.

AND Gate:

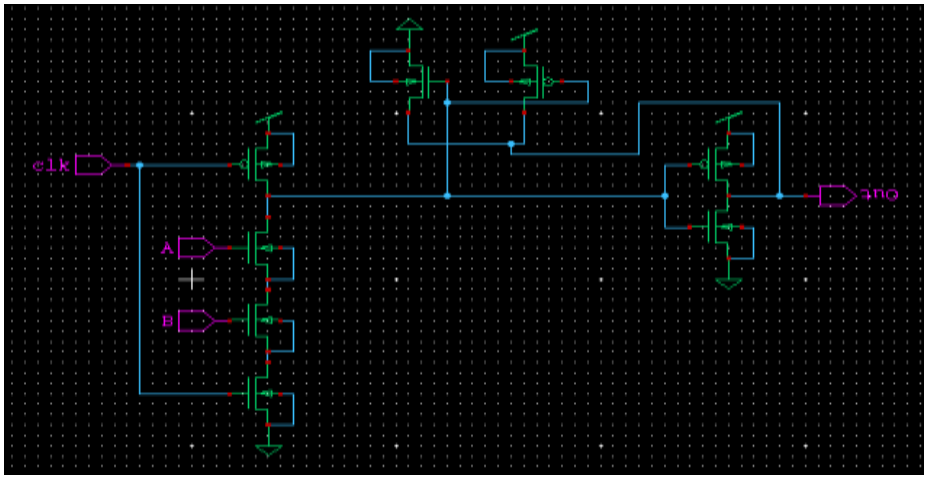

Fig 4

OR Gate:

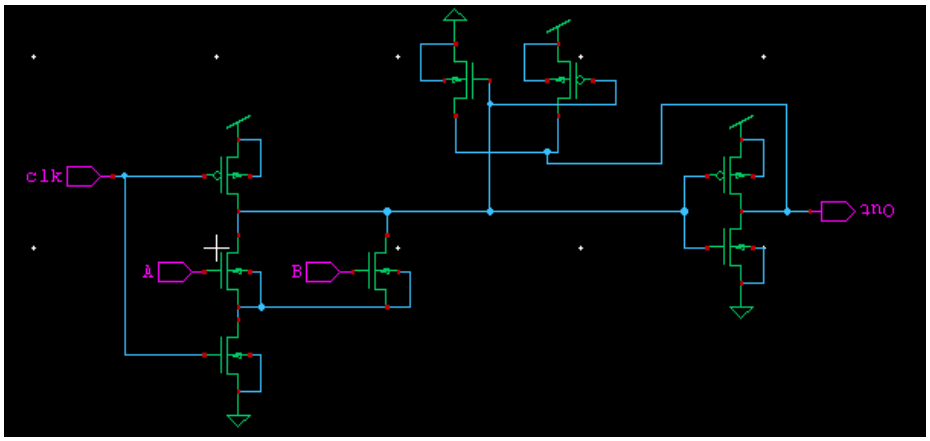

Fig 5

(D)HIGH SPEED MASTER OUTPUT KEEPER DOMINO TECHNIQUE-The speed of the circuit depends upon the time taken by the circuit to ground the all charge of the capacitance and time taken to charge the capacitance up to VDD. Thus to increase the speed of the circuit, we use an another path to ground the charge. Now there are two path to ground the charge, so the dischanging time reduced of the circuit and delay as well.
Case-1:When clock is LOW, NMOS m2 is OFF, so there is no path to ground the charge of capacitance. It is called PRECHARGE phase.
Case-2: In EVALUATION phase , When clock is HIGH , NMOS m2 is on .then dynamic node is ground or not , depends upon the NMOS PULL DOWN network.
A)When NMOS PULL DOWN network is ON, then the NMOS m1 is also ON, then there will be two paths to discharge the capacitance . Hence capacitance is discharge rapidly.thus delay of the circuit is reduced.
B) When NMOS PULL DOWN network is OFF, then NMOS m1 is also OFF, there will not be any path to discharge the capacitance .Hence the dynamioc node stuck at HIGH.

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Hence the delay problem is resolved by the HIGH SPEED MASTER OUTPUT KEEPER.
(i)AND gate:

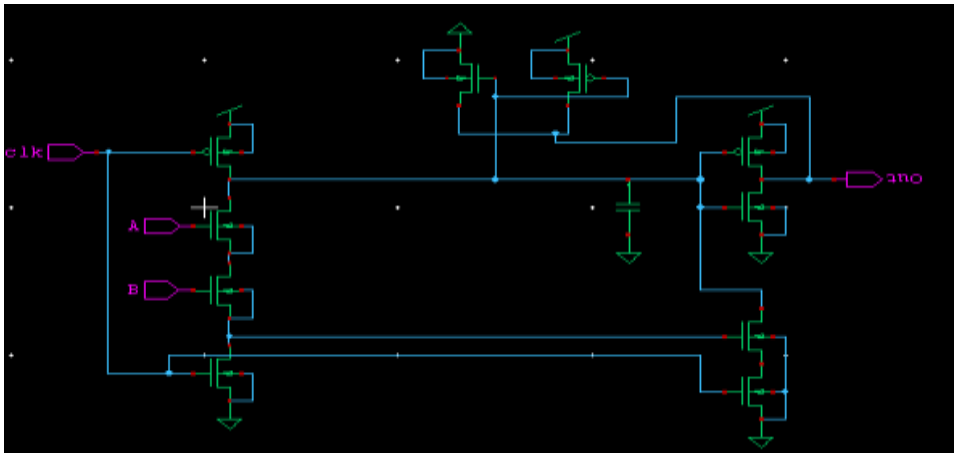

Fig 6

(ii)OR gate:

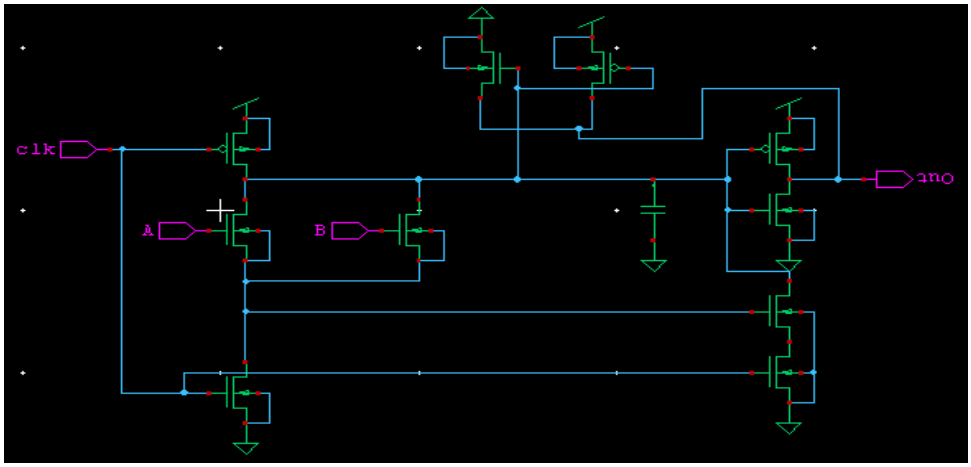

Fig 7

POWER DESSIPATION

The power consumed by CMOS circuit classified in two type:

- Static power dissipation
- Dynamic power dissipation

(a) Static Power Dissipation: This is the power dissipation due to leakage currents which flow through a transistor when no transaction occurs and transistor is in a steady state. Static power dissipation in CMOS inverter is negligible. Total static power consumption, P_s can be obtained as shown in equation .

$$P_s = \Sigma \text{ (leakage current)} \times \text{(supply voltage)}$$

(b) Dynamic Power Dissipation: The PMOS and NMOS transistors are on during the perform operation simultaneously. The duration of charging inputs low to high and discharging high to low PMOS and NMOS turn on respectively. During this time a current flows between Vdd to GND (make short path)and dynamic power produce. It is given by following equation:

$$P_T = C_{pd} \times V_{cc}^2 \times f_i \times N_{sw}$$

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Pt = transient power consumption ;V_{cc} = supply voltage ;F_l= input signal frequency ;N_{sw} = number of bits switching; C_{pd} = dynamic power-dissipation capacitance

PROPAGATION DELAY-

The propagation delay of a gate is the average transistor delay time for the signal to propagate from the input to output when the binary signal changes its value. . The average propagation-delay time is calculated as the average of the two delays t_{PHL} and t_{PLH} .

t_{PLH} : It is the propagation delay time in going from logic low to logical high .

t_{PHL} : It is the propagation delay time in going from logical high to logical low .

SIMULATION AND RESULT

In this work, the OR and AND logic gate had used for implementation of four techniques, in which third and fourth techniques are for reducing noise and delay of the circuit. Noise and delay are used to compare these techniques.

Table 1 contains all the simulation results of all four techniques.

Table 2 contains comparison of power(W) of all four techniques.

Table 3 contains comparison of delay (ns) of all four techniques.

Table 4 contains comparison of noise (nv/hz) of all four techniques.

From the result ,it can be observed that smart o/p keeper has less noise density than basic domino and domino with keeper but delay is increased. The delay is reduced by high speed master o/p keeper. Thus among four techniques , high speed master o/p keeper has less noise and delay.

Techniques	Circuit	Power(W)	Delay(ns)	Noise Density (nv/Hz)
1.Basic Domino logic	a. AND gate	2.965965e-001	12.30	1.89912
	b. OR gate	2.973454e-001	11.74	2.00478
2.Keeper Domino	a. AND gate	3.045195e-001	9.27	1.75407
	b .OR gate	3.040148e-001	6.82	1.79990
3. Smart o/p keeper	a. AND gate	3.034871e-001	15.45	1.41390
	b. OR gate	3.046125e-001	12.94	1.40291
4.High Speed Master o/p keeper	a. AND gate	3.007565e-001	9.79	1.42219
	b. OR gate	3.020864e -001	8.13	1.46140

Table 1

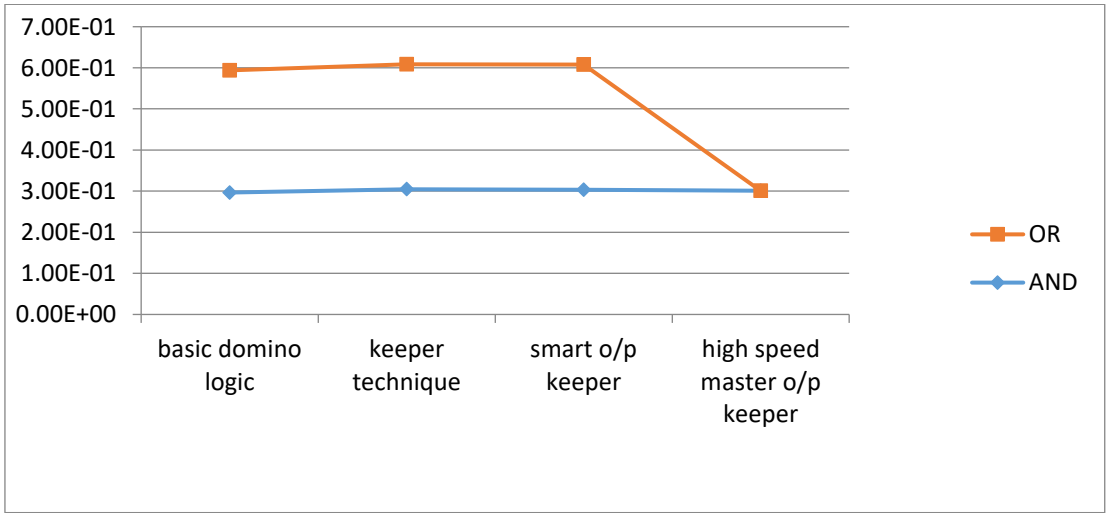

Table 2

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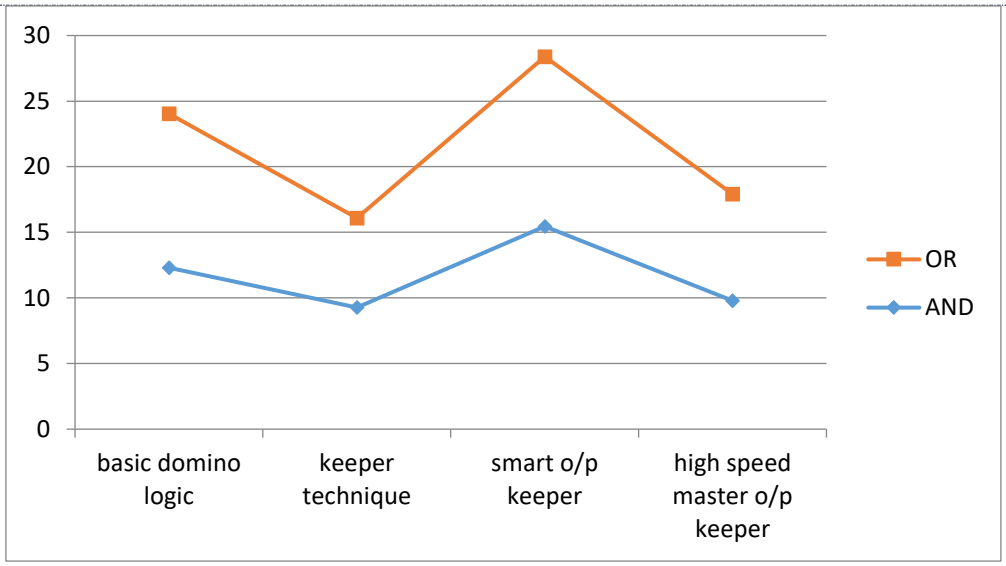

Table 3

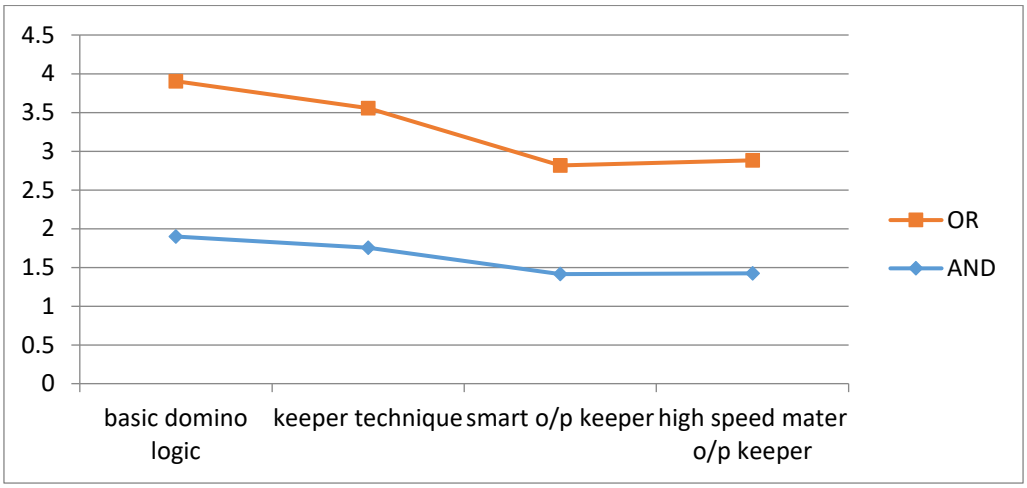

Table4

CONCLUSION

In this work, an attempt had been made to simulate OR and AND gate for all four techniques. Table 1 shows the results of simulation of all four techniques. Table 2 , Table 3 and Table 4 shows the comparison among different techniques for power dissipation, delay and noise density. High speed master o/p keeper is best techniques among four because it has better noise immunity and less delay.

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CITE AN ARTICLE:

Kumar, Ankit , and A.K. Gautam, Dr. "IMPROVEMENT IN NOISE AND DELAY IN DOMINO CMOS LOGIC CIRCUIT." *INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY* 6.5 (2017): 191-97. Web. 10 May 2017. <http://www.ijesrt.com/issues%20pdf%20file/Archive-2017/May-2017/26.pdf>